An Integrated GPS Receiver with Synthesizer and Downconversion Functions

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ABSTRACT

An integrated circuit for GPS (Global Positioning System) receivers has been developed which includes, on one chip, an L-band downconversion function, and an LO synthesizer function with a phased-locked loop. The downconversion function contains an L-Band amplifier, active mixer, and IF amplifier. The synthesizer function is comprised of a VCO, a prescaler, a phase/frequency detector, and loop amplifier. The chip also contains output buffers for three frequencies generated by the synthesizer, and on-chip power regulation. This IC advances the level of integration for IC's operating at the L-band frequencies used by GPS. This paper will report on the design, performance, packaging, and testing techniques.

INTRODUCTION

The successful integration of the front-end receiver functions into a single IC can lead to a major reduction in the cost, size, and power consumption of a Global Positioning System (GPS) receiver. This paper describes an IC design that advances the level of integration of reported receiver IC's at GPS frequencies by including on one chip downconversion and a phase locked LO synthesizer. [1][2]

A block diagram of the downconverter/ synthesizer chip is shown in Figure 1. The chip amplifies and downconverts the L-band GPS frequency of 1.575 GHz at a 50 ohm input to an IF frequency of 194 MHz at a balanced 200 ohm output. The LO is generated by an on-chip VCO designed to present a negative impedance to an external resonator/varactor to control the frequency. The LO is phase locked to a reference near 1.38 GHz with an on-chip divide-by 1080 prescaler and phase/frequency detector. The phase lock loop bandwidth is determined with off-chip RC components. On-chip band-gap reference and voltage regulation are used to supply power to the various functions.

DESIGN AND PERFORMANCE

The L-Band amplifier was designed to achieve simultaneously a good input noise match and power match to 50 ohms with no external tuning elements.

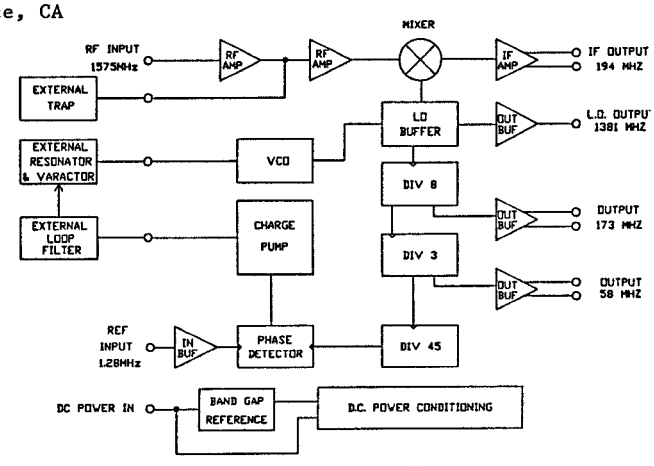

Figure 1. Block Diagram of Downconverter Synthesizer Chip

This was done by optimizing the phase and amplitude of a feedback signal to a common emitter stage. Typical receiver applications will use an external low noise preamplifier for several reasons: 1) A discrete single-stage amplifier can achieve a lower noise figure than obtainable with this integrated technology; 2) The external amplifier can be co-located with a remote antenna; 3) The image noise can be removed by controlling the bandwidth of the external amplifier. Therefore, the noise figure of the chip was not a critical factor. The design goal was to achieve a reasonable noise figure and VSWR without the use of external matching elements. An output port is supplied after the L-Band amplifier to accommodate an external shunt image trap to filter out the image noise. At the GPS L_1 frequency (1.575 GHz) the L-Band Amplifier has a noise figure of 4.5 dB. At the L_2 frequency (1.228 GHz) the noise figure is 3.9 dB as measured using the trap port as an output.

A four-quadrant mixer based on a Gilbert cell design is used for the downconversion. The IF amplifier was designed to drive a balanced 200 ohm output. Figure 2 displays the measured conversion gain for the upper and lower sidebands with a fixed LO of 1.381 GHz. A length of open transmission line was used at the trap port to reduce the gain of the lower sideband in order to to suppress the image noise.

An on-chip VCO is used to generate the LO for the downconversion. The VCO is designed to present

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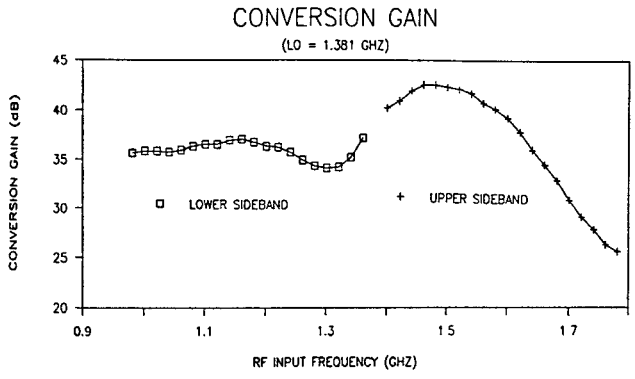

Figure 2. Conversion Gain with Fixed LO

a negative impedance to an external microstrip resonator loaded with a varactor diode for frequency control. The output of the VCO is buffered to drive the on-chip mixer, a 50 ohm output, and the prescaler.

The prescaler is used to phase-lock the VCO. It uses ECL master/slave flip-flops to divide the VCO frequency by a factor of 1080 for input to the phase detector. The prescaler is also used to drive output buffers to supply frequencies at one-eighth and one-twenty-fourth of the LO frequency for use elsewhere in the receiver system.

A digital Phase/frequency detector is used to generate an error voltage that is proportional to either the frequency or phase difference between the reference and prescaled VCO signal. This is done using ECL type circuits, arranged as in the logic diagram of Figure 3. The outputs of this

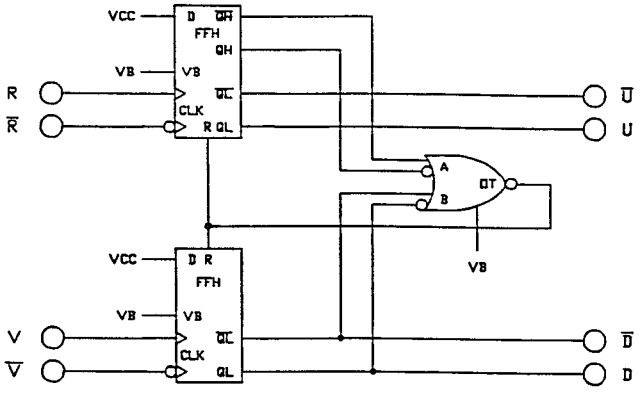

Figure 3. Logic Diagram of the Phase Detector

logic arrangement control a circuit which pumps current to or from an integrator. This produces a voltage to drive the VCO toward phase lock. Figure 4 displays the measured integrated output of the charge pump as a function of the phase difference between the reference and the output of the prescaler. A common criticism of this type of

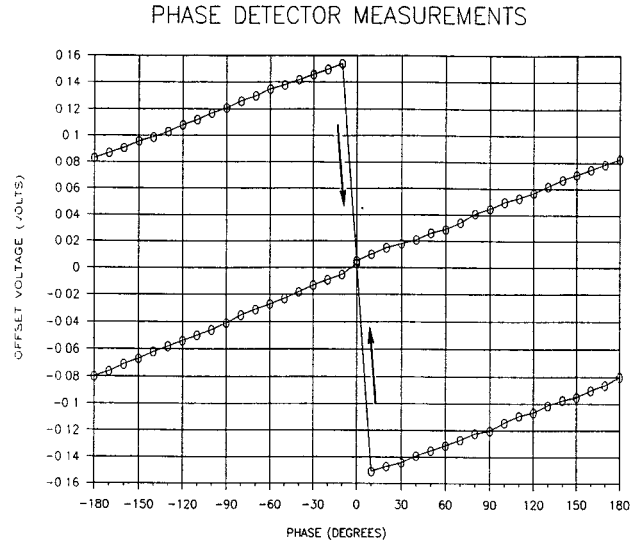

Figure 4. Error Voltage vs Phase Difference

phase detector is the possibility of a "dead-zone" in the operation between positive phase and negative phase. This dead zone creates a region where the phase detector is non-responsive to small phase errors. However, the actual operation of this type of phase detector as it goes through zero phase depends upon the details of the circuit design. Figure 5 displays the measured output near zero phase and indicates this circuit design produces a region of enhanced detector gain. Since the loop parameters can be easily chosen to be robust to changes in the loop gain, this region produces no undesired behavior. The loop bandwidth is determined by the time constant of the integrator which is set with external R-C elements.

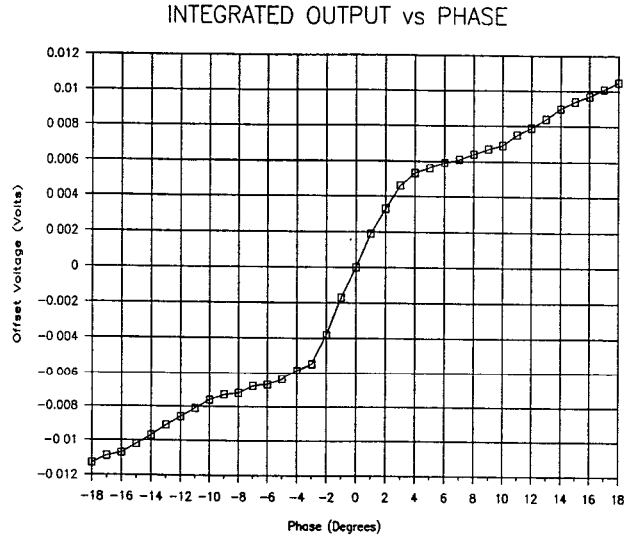

Figure 5. Error Voltage vs Phase Difference Near Zero

The phase noise of the LO is approximately -65 dBc/Hz at 25 Hz from the carrier as shown in Figure 6. This figure also displays the phase noise of the TCXO at 10.23 MHz. The TCXO was divided by 8 then used as the PLL reference. The arrow in Figure 6 indicates the theoretical contribution to the LO phase noise due to the TCXO because of the frequency ratio. Figure 6 indicates that the synthesizer does not significantly degrade the phase noise of the TCXO. The phase noise was measured using an in-house phase noise system which uses the error voltage of a calibrated phase locked loop as a detector.

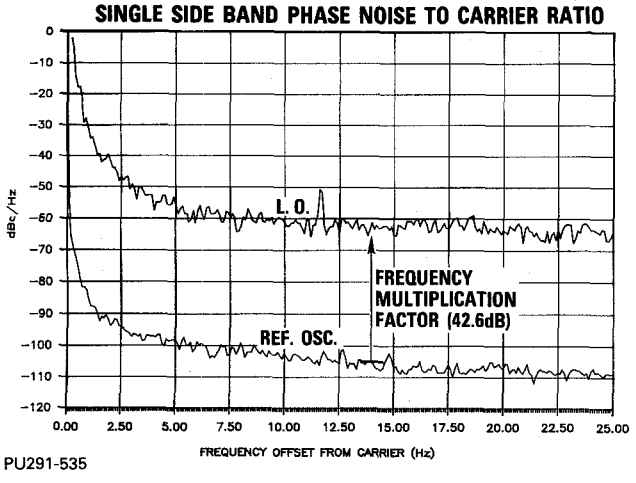

Figure 6. Phase Noise of LO and Ref. TCXO

The GPS receiver chip downconverts the low level GPS signals with up to 40 dB of conversion gain, while also processing high level digital signals in the synthesizer portion of the chip. Therefore, the isolation of signals between the different functions on the chip was a major requirement in the chip design. To meet this requirement, it was necessary to identify the various modes of crosstalk and then to control their effects. Crosstalk modes were associated with common power supply and ground impedances, mutual interconnect coupling (both on-chip and off-chip), substrate isolation, and internal circuit isolation. Figure 7 shows the levels of the spurs at the harmonics of the reference frequency as measured at the IF output. No attempt was made to filter the out-of-band spurs for this measurement. This measurement was made with the wide-band conversion response indicated in Figure 2. Using the L_1 conversion gain of 40 dB, the largest spur, other than the LO, is at LO/4 and has a level of -107 dBm referenced to the input of the chip.

FABRICATION

The chip was fabricated by Tektronix, using their SH-pi, full-custom foundry service. This is a silicon bipolar process that offers NPN transistors with a typical f_T of 8.5 GHz. A microphotograph of the RF downconverter-synthesizer

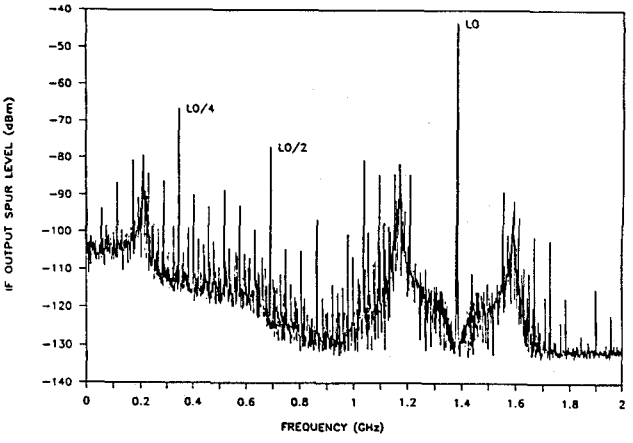

Figure 7. Spurious Response Measured at the IF Output

chip is shown in Figure 8. The chip measures 92 mils x 98 mills. The chip contains over 1400 circuit elements including over 800 transistors.

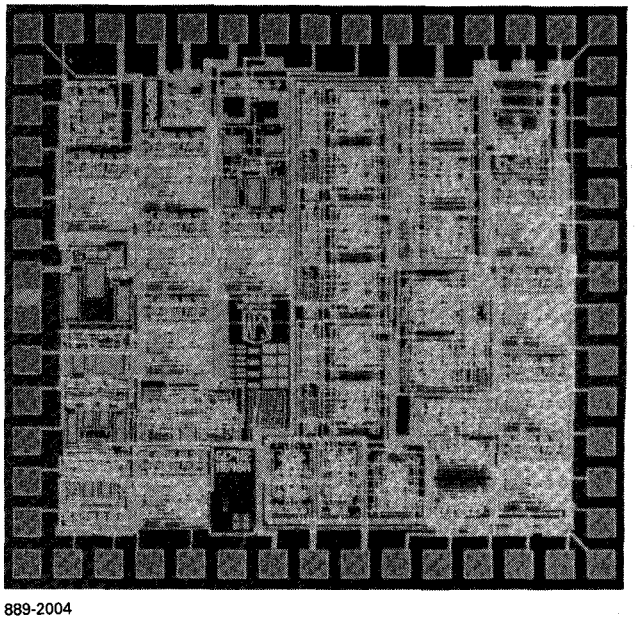

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Figure 8. Photomicrograph of GPS Receiver IC

PACKAGE AND WAFER TEST

The chip has been characterized on a test fixture as shown in Figure 9. This fixture brings controlled 50 ohm coplaner transmission lines to the chip to minimize the effects of unknown package parasitic. This IC has also been used successfully in GPS receivers in a variety of packages. Figure 10 is a photograph of the IC in a custom plastic package with the lid removed.

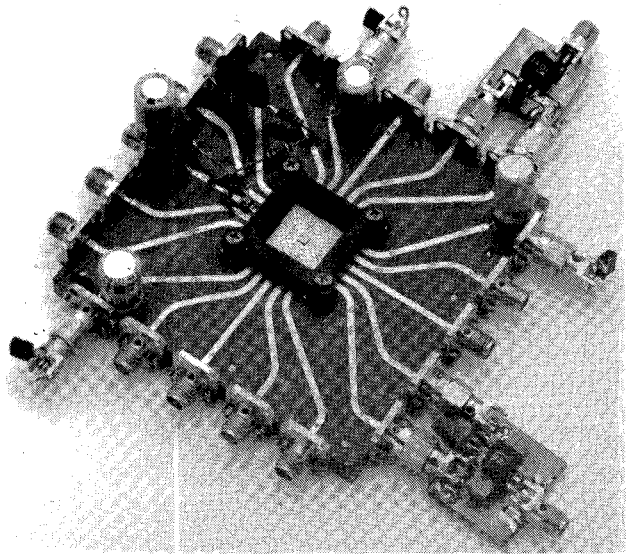

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Figure 9. Photo of Test Fixture

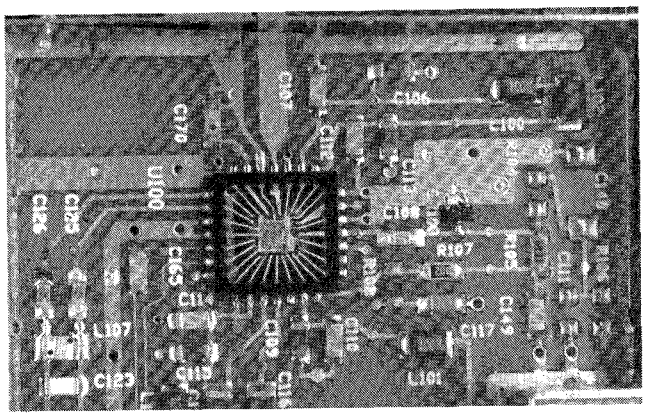

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Figure 10. Photo of Packaged Chip

The testing of high frequency ICs with high levels of integration can present problems, due to the high cost of custom RF test stations and the limited accessibility to the internal circuits. To achieve a low cost test, a wafer probe card (Figure 1) has been developed which fully exercises the chip at the operating frequencies, and interfaces to a low frequency (5 MHz) test station. The probe card contains this receiver IC in a package to generate the L-band frequencies used as inputs to the chip-under-test. The functionality of the chip-under-test is determined by monitoring DC and low frequency points with a standard IC test station. Figure 11 is a photograph of the custom wafer probe card.

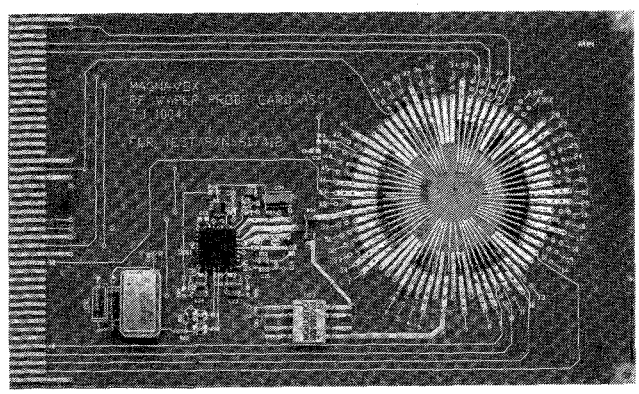

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Figure 11. Photo of Wafer Probe Card

CONCLUSION

The successful fabrication and demonstration of this GPS receiver IC indicates the practicality of high level integration at L-band frequencies. Sensitive analog receiver functions have been integrated with high speed digital functions. Excellent isolation has been achieved, resulting in low spurious response.

ACKNOWLEDGMENTS

We would like to thank Tektronix, Inc., for wafer fabrication and support with device modeling and design consultation.

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[1] R.M. Herman, et al, "A GPS Receiver with Synthesized Local Oscillator", ISSCC Digest of Technical Papers, p.194-195, Feb., 1989.

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